1-52223
AFOSR/NM
Dr Nachman

Final Report

for

Grant # F49620-96-1-0069

Analysis and Design of Mixed-Signal Electronic Packaging

for

the Period of

March 15, 1996 through December 31, 1998

Principal Investigator:

Lawrence Pileggi
Carnegie Mellon University
Department of ECE
5000 Forbes Avenue
Pittsburgh PA 15213
pileggi@ece.cmu.edu
412-268-6774

1.0 Objectives

As electronic systems continue to increase in complexity, the limits of single-chip capabilities are being reached and there are obvious economic and performance advantages to multi-chip module (MCM) solutions. This is particularly the case for mixed-signal systems, where analog and RF (radio frequency) circuits must be combined with digital processing circuits for applications such as portable wireless electronics. To design complex, multi-chip systems with the same efficacy afforded to today's integrated circuits (ICs) requires design automation algorithms and software that is presently unavailable. The objective of this project is to develop innovative algorithms and prototype tools that will help facilitate the design of mixed signal multi-chip modules and packaging in a manner that is similar to what is possible today for ICs.

One primary difference between a typical digital integrated circuit and a mixed-signal multi-chip electronic system is that magnetic coupling effects are just beginning to appear in ICs as giga-Hertz operating frequencies are approached, while they are a dominant influence on mixed-signal MCM performance. Unfortunately, modeling magnetic coupling effects (inductance) in electronic systems dramatically increases the design automation complexity. Moreover, because of the problem difficulty and the lack of impact on mainstream design in the past, inductance modeling capabilities have advanced much more slowly than many other similar design automation capabilities over the past few decades.

Advancing the modeling and analysis of inductance as it appears in electronic systems is one of the primary goals of this project. The proposed advances are considered on several fronts: 1) new algorithms and definitions for magnetic vector potentials which permit simplified inductance estimates for early phases of design; 2) Accurate 3-D inductance extraction algorithms that start with these inductance estimates and then adaptively grid the conductor materials as accuracy dictates; and 3) New automatic methods of model order reduction which generate provably passive, stable, and accurate representations of structures described by enormous large RLC (resistor-inductor-capacitor) circuits or discretized integral equations.

To demonstrate the utility of this modeling and extraction work, a second major planned goal of this project was to develop design automation algorithms that exploit these new found capabilities. The targeted prototype algorithms were: techniques for accurate power and ground noise modeling; signal integrity metrics based on RLC layout parameters; and package-level global placement and layout strategies. Because of the cut in funding to our program, we will not be able to explore these applications as part of this contract. Therefore, we are instead attempting to get our prototype modeling and extraction tools in the hands of electronic design engineers so that they can explore their use to control signal coupling and noise, tune the interconnect for optimal performance, and plan the package design like never before possible.

2.0 Status of Effort

We completed our objectives for developing new techniques for inductance extraction and macromodeling of large RLC equivalent circuit models. We have had extensive interactions with various companies with both the extraction and macromodeling prototype tools. Due to the fact that the final year of this contract was not funded, we moved some of the personnel onto other projects. As part of this process, the proposed work to do power/ground plane optimization was abandoned completely.

3.0 Accomplishments and New Findings

We made significant progress on fundamental concepts relating to extraction, modeling and analysis of RLC circuits. At CMU, a new algorithm for model order reduction using Arnoldi vectors and a congruence transformation was developed called PRIMA. PRIMA furthers the accuracy of the Arnoldi methods and along with stability also guarantees the model passivity. The PRIMA work has been incorporated in a prototype simulation and model order reduction tool, RICE5, and is already in use and under commercial development at several companies. PRIMA was used to simulate and perform model order reduction of a resistor-inductor coupled ground plane that included 185,000 components in approximately 6 CPU seconds, which was less than the time required to parse the circuit netlist.

In terms of partial inductance modeling we had previously proposed a new localized definition for magnetic vector potential based on assuming that return paths for currents are at a finite distance r0, rather than at infinity. Importantly, this work provided a provably stable approach to sparse partial inductance extraction. A CMU graduate student incorporated some of the results from this work in Hewlett Packard's commercial inductance extraction product. We further developed upper and lower bounds on the partial and self-loop inductances to establish a methodology for extracting only those mutual inductance terms that are important. Recently, we developed a new magnetic vector potential function model based on ellipsoid shells that provides increased accuracy and better bounding properties for general interconnect problems. A CMU graduate student is currently working at Intel to implement this model for on-chip inductance extraction. Sparse inductance extraction methodology being implemented by a CMU student at Intel Corporation and commercially developed at Pacific Numerics Corporation.

MIT's work on 3-D extraction, particularly adaptive gridding, was focused on using Sobolev-norm error estimates to drive adaptive refinement. The MIT team developed techniques for noncongruent panel refinement which automatically generates thin panels for edges starting from a uniform coarse discretization. In the area of fast analysis algorithms, they extended the precorrected-FFT electrostatic analysis algorithm to handle Green's functions associated with layered media. The FFTCAP tool for capacitance extraction is being considered for use by Ansoft and HP for their electromagnetic analysis tools. They also developed new integral equation multigrid method and applied it to analyzing substrate noise. The multigrid method is an order of magnitude faster than using GMRES plus sparsification. In the area of generating circuit models directly from 3-D analysis, they developed a mixed nodal-mesh formulation for electromagnetoquasistatic analysis (RLC) that is in the correct form to apply the multiple frequency point PRIMA model-order reduction algorithm. To make the approach efficient, they developed several new preconditioning strategies. This work was incorporated in the MIT inductance extraction tool, FastHenry, and is in use at Harris semiconductor and Intel.

4.0 Personnel Supported

Lawrence Pileggi, Professor, Carnegie Mellon University
Rob Rutenbar, Professor, Carnegie Mellon University
Jacob White, Associate Professor, Massachusetts Institute of Technology
Mustafa Celik, Research Associate, Carnegie Mellon University
John He, Research Assistant, PhD Student, Carnegie Mellon University
Altan Odabasioglu, Research Assistant, MS Student, Carnegie Mellon University
Michael Beattie, Research Assistant, PhD student, Carnegie Mellon University

Emrah Acar, Research Assistant, PhD student, Carnegie Mellon University
Johannes Tausch, PostDoc, Massachusetts Institute of Technology
Ibrahim El-fadel, Postdoc, Massachusetts Institute of Technology
Matt Kamon, PhD Student, Massachusetts Institute of Technology
Micheal Chou, PhD Student, Massachusetts Institute of Technology
Vivek Nadkarni, MS Student, Massachusetts Institute of Technology
Yehia Massoud, PhD Student, Massachusetts Institute of Technology
Jing-Rebecca Li, PhD Student, Massachusetts Institute of Technology
Junfeng Wang, PhD Student, Massachusetts Institute of Technology

5.0 Publications (which include citation of ARPA support)

A. Odabasioglu, M. Celik, L.T. Pileggi, PRIMA: Passive Reduced-order Interconnect Macromodeling Algorithm, *Proceedings of the International Conference on Computer-Aided Design, November* 1997.

Zhijiang (John) He and Lawrence T. Pileggi, A Simple Algorithm for Calculating Frequency-Dependent Inductance Bounds , Proceedings of the Custom Integrated Circuits Conference, May 1998.

M. Celik and L. T. Pileggi, Simulation of Lossy Multiconductor Transmission Lines Using Backward Euler, *IEEE Transactions on Circuits and Systems* I: Fundamental Theory and Applications, Vol. 45, No. 3, pp. 238-243, March 1998.

A. Odabasioglu, M. Celik and L. T. Pileggi, PRIMA: Passive Reduced-Order Interconnect Macromodeling Algorithm, *IEEE Transactions on Computer-Aided Design*, Vol. 17, No. 8, pp. 645-654, August 1998.

Rohini Gupta, John Willis and L.T. Pileggi, Analytic Termination Metrics for Pin-to-Pin Lossy Transmission Lines with Nonlinear Drivers, *IEEE Transactions on VLSI Systems*, Vol. 6, No. 3, pp. 457-463, September 1998.

M. Beattie and L. Pileggi, Equipotential Shells for Efficient Inductance Extraction, *Proceedings of the SRC Techcon Conference,* September 1998.

M. Beattie, L. Alatan and L. Pileggi, Equipotential Shells for Efficient Partial Inductance Extraction, *Proceedings of the International Electronics Devices Meeting,* December 1998.

M. Beattie and L. Pileggi, IC Analyses Including Extracted Inductance Models, *Proceedings of the Design Automation Conference*, Invited Paper, June 1999.

J. R. Phillips and J. K. White, "A Precorrected-FFT method for Electrostatic Analysis of Complicated 3-D Structures," IEEE Trans. on Computer-Aided Design, October 1997, Vol. 16, No. 10, pp. 1059-1072.

M. Chou and J.K. White, "Efficient Formulation and Model-Order Reduction for the Transient Simulation of Three-dimensional VLSI Interconnect", IEEE Trans. on Computer-Aided Design, December 1997, Vol. 16, no.12, pp. 1454-1476.

J. Wang and J. White, ''Fast Algorithms for Computing Electrostatic Geometric Sensitivities," Intl. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD), Boston, September, 1997, pp. 121-124.

J. Li and J. White, ''Approximation of Potentials by Multipole Grid Projections," Topical Meeting on Electrical Performance of Electronic Packaging, San Jose, California, November, 1997.

M. Kamon, N. Marques, and J. White, ''FastPep: A Fast Parasitic Extraction Program for Complex Three-Dimensional Geometries," Proceedings of the IEEE Conference on Computer-Aided Design, San Jose, November, 1997.

M. Kamon, N. Marques, L. Miguel Silveira and J. White, ''Generating Reduced Order Models via PEEC for Capturing Skin and Proximity Effects", Proceedings of the 6th Topical Meeting on Electrical Performance of Electronic Packaging, San Jose, California, November, 1997.

M. Chou and J. White, ''Multilevel Integral Equation Methods for the Extraction of Substrate Coupling Parameters in Mixed-Signal IC's," Proceedings of the 35th Design Automation Conference, San Francisco, June, 1998, pp. 20-25.

N. Marques, M. Kamon, J. White, L. M. Silveira, ''A Mixed Nodal-Mesh Formulation for Efficient Extraction and Passive Reduced-Order Modeling of 3D Interconnects,"Proceedings of the 35th Design Automation Conference, San Francisco, June, 1998, pp. 297-302.

Y. Massoud, S. Majors, T. Busami, and J. White, ''Layout Techiques for Minimizing On-Chip Interconnect Self Inductance," Proceedings of the 35th Design Automation Conference, San Francisco, June, 1998, pp. 566-571.

Y. Massoud and J. White, ''Fast Inductance Extraction of 3-D Structures with Non-constant Permeabilities,"International Conference on Modeling and Simulation of Microsystems, Semiconductors, Sensors and Actuators, Santa Clara, April 1998.

6.0 Interactions/Transitions

6.1 Meetings, Conferences and Seminars

DARPA, Washington DC, "Analysis and Design of Mixed-Signal Electronic Packaging," August 8, 1997.

International Conference on Computer-Aided Design. San Jose CA. PRIMA: Passive Reduced-order Interconnect Macromodeling Algorithm. November 1997.

Custom Integrated Circuits Conference. A Simple Algorithm for Calculating Frequency-Dependent Inductance Bounds. May 1998.

6.2 Consultation and Advisory Functions

Professor Pileggi has joined the technical advisory board of Coyote Systems, San Francisco CA.

6.3 Transitions

Intel, HP and IBM and several other companies are using the PRIMA software tool.

Intel and HP are currently evaluating the prototype implementation of the SPIE partial inductance tool.

Intel and Harris Semiconductor are using the MIT inductance extraction tool.

7.0 New Discoveries, Patents and Inventions

None.

8.0 Honors and Awards

Best paper award nomination from IEEE Trans. on CAD for the PRIMA publication.

X-Sender: kia@divine.eecs.berkeley.edu
X-Mailer: QUALCOMM Windows Eudora Pro Version 4.1
Date: Thu, 25 Mar 1999 14:35:20 -0800
To: zanger@cs.cmu.edu, msk@ece.cmu.edu, ann@cs.ucla.edu, lisa@ece.ucsb.edu
From: Kia Cooper <kia@eecs.berkeley.edu>
Subject: URGENT!! MARCO/DARPA Request - I need your info. ASAP!!
Cc: maly@ece.cmu.edu, pileggi@ece.cmu.edu, cong@cs.ucla.edu, abk@cs.ucla.edu,
rnewton@ic.eecs.berkeley.edu, timcheng@ece.ucsb.edu, mms@ece.ucsb.edu

Hello All,
I really need this info. ASAP.
Your information is the only outstanding info. I need to submit my report
to DARPA by tomorrow morning.
Thanks,
Kia

>Date: Tue, 23 Mar 1999 15:14:37 -0800
>To: chapman@eecs.umich.edu, cathy@ee.princeton.edu,
>tran@forsythe.stanford.edu, zanger@cs.cmu.edu, msk@ece.cmu.edu,
>tlow@lcs.mit.edu, attari@ece.ucsd.edu, ann@cs.ucla.edu, lisa@ece.ucsb.edu,
>lisa@cse.ucsc.edu, down@cse.ucsc.edu
>From: Kia Cooper <kia@eecs.berkeley.edu>
>Subject: URGENT Request!! MARCO/DARPA GSRC Contract
>Cc: rnewton@ic, hodges@eecs.berkeley.edu, elise@eecs.berkeley.edu,
>deirdre@eecs.berkeley.edu
>
>Hello All,
>My apologies for yet another URGENT request. This afternoon I received a
>request from
>DARPA to report on the GSRC expenses to date and your forecasted expenses
>for the term of the contract.
>
>1. Pls. send me a monthly breakdown of the total costs you've expended since
>10/1/98 through now (ie. 10/98 25k, 11/98 10k etc).
>
>2. Pls. send me the total costs for your forecasted budgets for the
>following time periods:
>   Year 1: 10/98-12/31/99
>   Year 2: 1/00-12/31/00
>   Year 3: 1/01-12/01
>   Pls. note the funds from Yr 1 will roll over to Yr 2 in your subcontract
>but you should still plan to spend as much of the Yr 1
>   funds in Yr 1 even though your subcontracts weren't officially in place
>until recently. If your University's acctg. system doesn't
>   allow for you to retroactively charge your subcontract then pls. let me
>know your plan to spend the funds.
>
>DARPA is okay with the fact that these will be unofficial numbers so its
>best that you overestimate the funds
>that you've expended vs underestimating.

REPORT DOCUMENTATION PAGE

AFRL-SR-BL-TR-00-

0177

8

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 1999	Final Technical Report 15 Mar 96 to 31 Dec 98

4. TITLE AND SUBTITLE
Analysis and Design of Mixed-Signal Electronic Packaging

5. FUNDING NUMBERS
F49620-96-1-0069

6. AUTHOR(S)
Professor Lawrence Pileggi

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Carnegie Mellon University
Department of ECE
5000 Forbes Avenue
Pittsburgh PA 15213

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NM
801 N. Randolph St, Rm 732
Arlington, VA 22203-1977

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
F49620-96-1-0069

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The objective of this project is to develop innovative algorithms and prototype tools that will help facilitate the design of mixed signal multi-chip modules and packaging in a manner that is similar to what is possible today for ICs.
The proposed advances are considered on several fronts: 1) new algorithms and definitions for magnetic vector potentials which permit simplified inductance estimates for early phases of design; 2) Accurate 3-D inductance extraction algorithms that start with these inductance estimates and then adaptively grid the conductor materials as accuracy dictates; and 3) New automatic methods of model order reduction which generate provably passive, stable, and accurate representations of structures described by enormous large RLC (resistor-inductor-capacitor) circuits or discretized integral equations.

14. SUBJECT TERMS	15. NUMBER OF PAGES	16. PRICE CODE
	7	

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL